	L #	Hits	Search Text	DBs	Time Stamp
1	L1	2276	(438/622).CCLS.	4	
2	L2	2142	(438/637).CCLS.		
3	<b>L</b> 3	751	(438/638).CCLS.	I	·
4	L4	916	(438/723).CCLS.		
5	L5	500	(438/724).CCLS.		

	L	#	Hits	Search Text	DBs	Time Stamp
6	L6		16	("6297162") or ("6225207") or ("5162258") or ("5792704") or ("5972192") or ("5990015") or		
7	Ъ7		2	("6329234").PN.	1	
8	L8		14	("5194932"   "5208726"   "5293510"   "5406447"   "5675184"   "5726083"   "5879985"   "5932906"   "5946569"   "5998276"   "6146941"   "6184076"   "6258653"   "6259128").PN.	PGPUB;	2005/01/20 14:00
9	Ь9		25	("6329234").URPN.	RISPAT	2005/01/20 14:20
10	L10	)	2199	(metal-insulator-Metal or (metal near insulat\$6 near metal)		

	L #	Hits	Search Text	DBs	Time Stamp
11	L11 ·		"etch stop" or "etch stopper" or ((stop\$4 or barrier) near4	l .	
12	L12	430	10 and 11		
13	L13	226	12 and (copper or Cu)		
14	L14	53	13 and ((@ad<"20010104") or (@rlad<"20010104"))		2005/01/20 14:25

US-PAT-NO: 6759703

DOCUMENT-IDENTIFIER: US 6759703 B1

TITLE: Capacitor and a manufacturing process therefor

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Abstract Text - ABTX (1):

A capacitor has a coupled of electrodes with a dielectric placed therebetween. At least one of the electrodes is made of <u>copper</u>, and barriers

for preventing the diffusion of  $\underline{\text{copper}}$  into the dielectric are provided between

the dielectric and the copper electrodes, respectively.

Application Filing Date - AD (1): 20001011

Brief Summary Text - BSTX (5):

As one of prior arts for speeding up the operation of an integrated circuit,

which uses a unipolar transistor, such as a MOS transistor, or a bipolar

transistor, the so-called <u>copper</u> wiring technology is well known which uses

copper with lower electric resistance than aluminum to build circuit
wiring

previously formed by aluminum.

Brief Summary Text - BSTX (6):

Regarding the capacitor used in an integrated circuit, it is known that a

MIM (<u>Metal-Insulator-Metal</u>) capacitor is superior in high-frequency characteristics and more advantageous for improving the high-speed operation

properties of the circuit than the so-called PIP

(Polysilicon-Insulator-Polysilicon) capacitor in which a couple of electrodes

having a dielectric between them are made of a conductive polysilicon.

Brief Summary Text - BSTX (7):

It is also well known that it becomes possible to further improve the

high-frequency characteristics of the integrated circuit by combining the

above-mentioned copper wiring technology and technology for forming

the

electrodes of the  $\underline{\texttt{MIM capacitor}}$  not by aluminum but by a  $\underline{\texttt{copper}}$  metal material

with lower electric resistance than aluminum.

Brief Summary Text - BSTX (8):

However, the use of  $\underline{\text{copper}}$  for the electrodes of the  $\underline{\text{MIM capacitor}}$  as

mentioned above gives rise to a phenomenon that part of the copper
atoms

constituting the electrodes diffuse into the dielectric made of silicon oxide,

for example, between the electrodes of the capacitor. The diffusion of copper

atoms into the dielectric deteriorates the insulation characteristics of the

dielectric, and therefore decreases the dielectric property and the durability

of the capacitor.

Brief Summary Text - BSTX (9):

Furthermore, in shaping of the <u>copper</u> electrodes, it has been impossible to

apply etching technology, which is used on the aluminum electrode, and

therefore it has been difficult to form the <u>copper</u> electrodes in desired shape.

Brief Summary Text - BSTX (12):

According to a first aspect of a capacitor of the present invention, the

capacitor having a couple of electrodes with a dielectric placed therebetween,

at least one of the couple of electrodes being made of copper,
wherein the one

electrode and the dielectric, a barrier is provided to prevent diffusion of

copper into the dielectric.

Brief Summary Text - BSTX (14):

The barrier effectively prevents the diffusion of <a href="copper">copper</a> atoms from the

<u>copper</u> electrode into the dielectric, and therefore prevents the pollution of

the dielectric by the copper electrode and effectively prevents a
decrease in

the insulating properties of the dielectric by the pollution mentioned above.

Brief Summary Text - BSTX (15):

possible to make

good use of the advantage of using <u>copper</u> for the upper and the lower electrodes 17 and 20.

Detailed Description Text - DETX (27):

As shown in FIG. 2(a), an interlayer insulating film 13 is formed on the

semiconductor substrate 12 (not shown), and a SiN film 15a to serve as an

etching stopper film is formed on the interlayer insulating film. Though this

is not shown, a through-hole leading to the circuit portion under the interlayer insulating film 13 is formed, when necessary, in the SiN film 15a

and the interlayer insulating film 13.

Detailed Description Text - DETX (28):

Thereafter, a lower layer 14a of the interlayer insulating film 14 is

formed, and the lower insulating portion 14a is etched by a well-known

photolithographic etching technique using resist patterns (not shown on the

layer 14a) and etching to form a recess 24 and a trench 25 for the lower

electrode 17 and the lower wiring pattern 16a. In etching of the lower

insulating portion 14a for the recess 24 and the trench 25, because the SiN

film acts as an etching stopper film, the interlayer insulating film 13 under

the SiN film 15a is protected from the etching process.

Detailed Description Text - DETX (29):

TiN or TaN , which is a conductive material as mentioned above, is deposited

on all surfaces, including the surfaces of the recess 24 and the trench 25 and

the surfaces of the lower insulating film 14a by sputtering. The deposited

material is removed from the surface of the lower <u>insulating layer</u> where it is

not required, with the result that a barrier layer 18a is formed on the walls

of the recess 24 and the trench 25 as shown in FIG. 2(b).

Detailed Description Text - DETX (30):

The barrier layer 18a is made of a conductive material as described above.

and by electroplating using this conductive material as the seed

layer, a

copper material is deposited in the recess 24 and the trench 25,
which are

gradually filled with <a href="copper">copper</a>. The unwanted portion of the <a href="copper">copper</a> material

protruding from the surface of the lower insulating layer 14a is removed by

chemical mechanical polishing (CMP), and the lower electrode 17 and the lower

wiring pattern 16a are formed in the recess 24 and the trench 25 with interposition of the barrier layer 18a as shown in FIG. 2(b).

Detailed Description Text - DETX (33):

Referring to FIG. 2(d), a SiN film 15b just like the SiN film 15a is formed

on the surfaces of the lower <u>insulating layer 14a, the barrier</u> 18b and the

lower wiring pattern 16a, and an intermediate insulating layer 14b is deposited

on the SiN film 15b. A stepped portion is formed, which corresponds to the

peripheral edge portion of the barrier 18b, on the top surface of the intermediate insulating layer 14b, but it is removed by a well-known flattening

process. Thus, the top surface of the intermediate insulating layer 14b is

made flat as shown in FIG. 2(d). A SiN film 15c is formed on the top surface

of the flat intermediate insulating layer 14b.

Detailed Description Text - DETX (38):

After this, as shown in FIG. 2(e), the upper insulating layer 14c is etched

by photolithography and etching in the same manner as mentioned above, to

create trenches 28 and 29 for the wiring pattern 22 and the upper wiring

pattern 16c, respectively. A nitrided metal film 18c is formed by sputtering

in the same manner as mentioned above on the walls of the recess 19 and the

trenches 28 and 29. By electroplating using the nitrided metal film 18c as the

seed layer, <u>copper</u> is deposited in the recess 19 and the trenches 28 and 29,

and an excess portion of the <u>copper</u> is removed by CMP. In this manner, the

upper electrode 21, the wiring pattern 22 and the upper wiring pattern 16c all

made of copper are formed and as the result, the integrated circuit

Detailed Description Text - DETX (49):

Therefore, the capacitor electrode 17 and the wiring patterns 22 and 31 can

be formed of <u>copper</u> superior in conductivity without incurring the deterioration in insulating properties caused by <u>copper</u> atoms being diffused

into the interlayer insulating film 14, making it possible to improve the

high-frequency characteristics of the integrated circuit.

Detailed Description Text - DETX (51):

In FIG. 4(a), as shown in FIG. 2(c), a lower layer 14a of the interlayer

insulating film 14 is deposited on the SiN film 15a on the interlayer insulating film 13. The lower electrode 17 and the lower wiring pattern 16a,

both made of <u>copper</u>, are embedded in the lower <u>insulating layer 14a</u> with

interposition of the barrier 18a by carrying out the same procedure as

described with reference to FIG. 2. In addition, a barrier 18b is formed to

cover the exposed lower electrode 17.

Detailed Description Text - DETX (52):

As shown in FIG. 4(b), after the barrier 18b is formed, a SiN film 15b is

formed to cover the exposed surfaces of the <u>barrier 18b</u> and the <u>lower</u> insulating layer 14a, and an intermediate layer 14b of the interlayer insulating film 14 is deposited on the SiN film 15b.

Detailed Description Text - DETX (58):

According to the process shown in FIG. 4, the <u>barrier for</u> preventing the

decrease in insulating properties of the insulating film caused by copper metal

can be utilized as the seed layer in <a href="copper">copper</a> plating, so that it is possible to

efficiently form an integrated circuit 11, including a capacitor 10 shown in

FIG. 3, which is excellent in high-frequency characteristics and which has a

wiring pattern 31 above the upper electrode 30, without incurring the deterioration of the insulating film caused by copper metal.

Detailed Description Text - DETX (61):

In the capacitor 10 in the third embodiment shown in FIG. 5, instead of the

upper electrode 30 of tungsten as shown in the second embodiment, an upper

electrode 33 of a nitrided metal showing conductivity, such as a TiN film, is

used. The upper electrode 33 made of a nitrided metal is higher in electric

resistance than tungsten or <u>copper</u> mentioned above, and to reduce the resistance, a plurality of studs 34 are provided between the upper electrode 33

and the wiring pattern 31.

Detailed Description Text - DETX (64):

A lower insulating layer 14a is deposited on the SiN film 15a as the etching

stopper on the interlayer insulating film 13. The lower electrode 17
and the

lower wiring pattern 16a, both of <u>copper</u>, are embedded in the lower insulating

layer 14a with interposition of the barrier 18a by the same procedure as has

been described referring to the second embodiment. The flattening process is

carried out on the top surface of the upper insulating layer 14a in which the

lower electrode 17 and the lower wiring pattern 16a have been embedded.

Detailed Description Text - DETX (65):

As shown in FIG. 6(b), a nitrided metal layer for the barrier 18b is formed

by sputtering on the top surface of the flattened lower insulating layer 14a.

Moreover, the above-mentioned insulating film to serve as the dielectric is

formed on the nitrided metal layer 18d by CVD. Being formed on the flat

barrier layer 18b, the insulating film (20) becomes a flat plate with a

substantially uniform thickness.

Detailed Description Text - DETX (68):

Subsequently, as shown in FIG. 6(d), the SiN film 15b to serve as the

etching stopper and the intermediate insulating layer 14b are deposited, and

after a flattening process is carried out on the top surface of the intermediate insulating layer 14b, a SiN film 15c is formed, which is the same

as the one mentioned above.

Detailed Description Text - DETX (74):

According to the method shown in FIG. 4, as in the second

embodiment.

because the <u>barrier that prevents the deterioration of the insulating</u> films

caused by <a href="copper">copper</a> metal can be utilized as the seed layer in <a href="copper">copper</a> plating, an

integrated circuit 11 excellent in high-frequency characteristics and having

the wiring pattern 31 provided on the upper electrode can be formed efficiently

without incurring the deterioration of the insulating film ascribable to the

diffusion of copper atoms.

Detailed Description Text - DETX (81):

As shown in FIG. 4(a) showing the manufacturing process of the capacitor 10

of the second embodiment, in the second embodiment, to form the barrier 18b on

the lower insulating layer 14a, a nitrided metal layer (18b) is deposited

covering all over the top surface of the lower insulating layer 14a, then the

nitrided metal layer is patterned by photolithography and etching to remove the

unnecessary portions of the nitrided metal layer, so that the barrier layer 18b

is formed.

Detailed Description Text - DETX (84):

On the other hand, in the fourth embodiment, as shown in FIG. 8 depicting

the manufacturing process, a lower layer 14a of the interlayer insulating film

14 is deposited on the SiN film 15a as the etching <u>stopper film on</u> the

interlayer insulating film 13, and the lower electrode 17 and the
lower wiring

pattern 16a, both made of <u>copper</u>, are embedded in the lower <u>insulating layer</u>

14a with interposition of the barrier 18a by the same steps as described in the

second embodiment. After this, the top surface of the lower insulating layer

14a is subjected to the flattening process.

Detailed Description Text - DETX (85):

After the flattening process is finished, a SiN film 15b to serve as the

etching stopper film is deposited on the whole surface of the lower insulating

film 14a. Therefore, the SiN film 15b does not penetrate into any of the lower

insulating layer 14a, the lower wiring pattern 16a and the barrier layer 18a,

and the lower wiring pattern 16a and the <u>barrier layer 18b in the</u> lower

<u>insulating</u> layer 14a are covered with the SiN film 15b having a flat lower surface.

Detailed Description Text - DETX (89):

As described with reference to the second embodiment, on the SiN film 15b

and the <u>barrier layer 18b</u>, <u>an intermediate insulating</u> layer 14b and a SiN film

15c are deposited, then an upper electrode 30 partially covered with a nitrided

metal layer 18d and the studs 23 and 16b are formed. After this, an upper

insulating layer 14c is formed on the SiN film 15c, and the capacitor 10 is

completed by forming wiring patterns 31 and 22 and the upper wiring pattern 16c

on the upper insulating layer 14c.

Detailed Description Text - DETX (92):

According to the capacitor in the present invention, as described above, the

barrier that intervenes between the <u>copper</u> electrode and the dielectric

securely prevents <u>copper</u> atoms from diffusing from the <u>copper</u> electrode into

the dielectric, which prevents a decrease in electric resistance of the

dielectric polluted by <u>copper</u>, and therefore prevents the deterioration of the

capacitor by pollution by diffused **copper** atoms, which makes it possible to

improve the durability of the capacitor excellent in high-frequency characteristics.

Detailed Description Text - DETX (93):

According to the manufacturing process of the capacitor according

present invention, as has been described, at least one electrode made of copper

is formed by electroplating using the underlying nitrided metal film as the

seed, and therefore by forming the nitrided metal film in a desired shape, the

electrode can be formed in the desired shape of the nitrided metal film, and it

becomes relatively easy to form the capacitor superior in high-frequency

characteristics, including a copper electrode of desired shape.

## Claims Text - CLTX (1):

1. A capacitor formed on a substrate, having an upper electrode, and a

lower electrode interposed between the upper electrode and the substrate, with

a dielectric between the upper and lower electrodes, at least the lower

electrode being made of <u>copper</u>, wherein the lower electrode is formed in a

first recess that passes through a first insulating layer of an interlayer

insulating film, wherein top surfaces of the lower electrode and the first

insulating layer are formed along a first plane, the upper electrode and the

dielectric are formed in a second recess which passes through a second

insulating layer of the interlayer <u>insulating film</u>, a barrier is provided at a

top surface of the lower electrode to prevent diffusion of <a href="copper">copper</a> into said

dielectric, the lower electrode does not extend into the second recess, and the

dielectric extends out of the second recess on the top surface of the second

insulating layer, and wherein, a top surface of the dielectric on the second

insulating layer and a top surface of the upper electrode are coplanar.

## Claims Text - CLTX (2):

2. A capacitor according to claim 1, wherein the upper electrode is also

made of <u>copper</u>, wherein between said upper electrode and said dielectric a

second barrier is provided to prevent diffusion of <u>copper</u> into said dielectric.

## Claims Text - CLTX (10):

10. A capacitor according to claim 9, wherein said wiring pattern is made

of <u>copper</u> and a second <u>barrier is provided between said wiring</u> pattern and said

insulating layer to prevent diffusion of copper into said insulating